REMARKS

Applicant respectfully requests reconsideration and allowance in view of the foregoing amendements and the following remarks. Applicant notes that claims 1 and 12 have been amended. Thus, claims 1-21 are pending in the application.

Claim Objections:

In the Office Action, claims 1-21 were objected to because claim 1 failed to comply with the requirement that the text of any added subject matter must be shown by underlying the text. Applicant has amended claim 1 to correct the noted informality. Therefore, Applicant respectfully requests that the claim objections with respect to claims 1-21 be withdrawn.

Section 112 Rejections:

In the Office Action, claims 1-21 were rejected under 35 USC 112, first paragraph, for failing to comply with the written description requirement. Specifically, the Office Action alleged that the limitation "wherein the signal-generating unit (40) and the evaluation unit (70) are integral parts of the integrated circuit" as recited in claim 1 was not described in the specification in such a way as to reasonably convey that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant respectfully traverses the Section 112, first paragraph, rejections. In particular, Applicant points to page 4, lines 9-16, which states "[i]n summary, it can be concluded that the present invention provides an electric or electronic circuit arrangement as well as a method of protecting an electric or electronic circuit arrangement from manipulation and/or abuse in which . . . a complete integration of the envisaged 'capacitive detector' in the (semiconductor) chip is possible without electric connections to the exterior – possibly via contact pads – being required and independent of the fact how the (semiconductor) chip is eventually used." Because the electric circuit arrangement and/or capacitive detector provided by the present invention and referred to the in the cited passage includes a signal-generation unit and evaluation unit (see page 3, lines 23-26; and page 3, line 33 – page 4, line 8), Applicant respectfully submits that the specification indicates that the signal generation unit and evaluation unit can be completely integrated in the semiconductor chip. In fact, this may be the only way to implement the envisaged capacitive detector without electric connections to the exterior of the semiconductor chip as also referenced in the cited passage.

The Office Action, however, appears to suggest that page 1, lines 1-9, page 5, lines 14-20 and Figures 1 and 2 show that the signal-generation unit 40 and evaluation unit 70 are external to the integrated circuit. Applicant respectfully submits that this interpretation is inconsistent with the cited passage above and misconstrues the features illustrated and described with respect to Figures 1 and 2. For example, the Office Action appears to suggest that layered carrier substrate 10 illustrated in Figure 2 constitutes the metes and bounds of the semiconductor chip. Applicant respectfully disagrees and submits that the layered carrier substrate 10 illustrates the features of the parallel conducting tracks 20, 25, a cross-section of which is illustrated in Figure 1. In this context, the layered carrier substrate 10 in Figure 2 provides a convenient cross-reference for showing the cross-section of the layered carrier substrate 10 in Figure 1. Furthermore, if the interpretation used in the Office Action were applied, this interpretation would require the contacts 22 and 27 illustrated in Figure 2 to provide exterior electric connections, which the passages discussed above the preceding paragraph specifically state would not be required by embodiments of the present invention. Instead, Applicant respectfully submits that the electric circuit arrangement 100 illustrated in Figure 2 shows the circuit arrangement that can be potentially integrated in a semiconductor chip without requiring exterior electric contacts.

Therefore, in view of the foregoing remarks, Applicant respectfully requests that the Section 112, first paragraph, rejections with respect to claims 1-21 be withdrawn.

Section 102/103 Rejections:

In the Office Action claims 1, 2 and 6-21 were rejected under 35 USC 102(b) as being anticipated by Hierold (DE 19738990A1) and claims 3-5 were under 35 USC 103(a) as being unpatenable over Heirold.

With regard to independent claims 1 and 12, Applicant notes that these claims recite that the signal-generating unit (40) and the evaluation unit (70) are provided as integral parts of the integrated circuit. The Office Action specifically did not address these features of the claimed invention in view of the Section 112, first paragraph, rejections. Because Applicant respectfully submits that the foregoing remarks overcome the Section 112, first paragraph, rejections, Applicant respectfully submits that claims 1 and 12 also define over Heirold, since Heirold fails to teach or suggest these aspects of the claimed invention for at least the reasons discussed in the Reply dated October 17, 2003. Therefore, Applicant respectfully requests that the Section

102/103 rejections with respect to claims 1 and 12 and all claims dependent thereon be withdrawn.

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-21 are in condition for allowance. Applicant, accordingly, respectfully requests that a notice of allowance be issued with respect to claims 1-21.

Please charge any fees which may be required, except the issue fee, or credit any overpayment to Deposit Account No. 14-1270.

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Respectfully submitted,

By _____

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